REMARKS

In the Office Action mailed on May 15, 2007, the Examiner rejected claims 28-30 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,128,467 to Rege in view of U.S. Patent No. 5,619,528 to Rebec and U.S. Patent No. 6,342,921 to Yamaguchi and rejected claims 31 and 32 under 35 U.S.C. 103(a) as being unpatentable over Rege, Rebec and Yamaguchi in view of U.S. Patent No. 7,127,736 to Kondo.

In response, Applicant has amended claim 28 and added new claim 33. No new matter has been added.

The Examiner argues that Rege teaches the CPU 310 serializing the encoded content in column 6, lines 47-54. Applicant disagrees. Column 6, lines 47-54 do discuss receiving data, presumably from the disks, sequentially. This passage goes on to state that if the viewer wishes to watch the content out of order (e.g., skip certain portions), the content is retrieved from the disk out of normal sequential order. This is not what is claimed in claim 28. Instead, claim 28 Independent claim 28 is directed to organizing the data for transportation over the physical layer. In claim 28, if a viewer were to skip a section of content, those portions of the content that are sent to the viewer would still be serialized by the media interface module. Thus, Rege describes receving portions of content out of sequential order, while claim 28 pertains to serializing the portions of content transmitted to the user, whether those portions are sent to the user in sequential order or not.

Amended claim 28 also recites a backplane interface that is used to input content into the semiconductor memory. Rege uses the servers 300 for both inputting data into the disks and outputting data from the disks. See column 3, line 66 – column 4, line 1.

Rege does not have a dedicated piece of hardware, such as the claimed backplane interface, for inputting data into the disk array. Thus, Rege does not teach or suggest a backplane interface.

In addition, the Examiner asserts that Rege shows an address bus in Fig. 4. Applicant again disagrees. In semiconductor memory, an address bus is a control bus used to select one or more locations within the memory for reading from or writing data into the memory. Thus, the address bus is coupled to and part of the semiconductor memory. Rege's lines 403 are control lines in that the control the switch elements 500 to connect and disconnect vertical lines 401 from servers 300 with horizontal lines 402 from disks 800. See column 3, line 66 – column 4, line 1. Control lines 403 are therefore not coupled to nor are they are a part of disks 800. Control lines 403 do not control which portions of data to output from disks 800. Thus, Rege does not show an address bus in Fig. 4 as asserted by the Examiner. It should also be noted that Rege does not describe any lines 403 being grouped into quantities bigger than 32 bits.

The Examiner also replaces the disks of Rege with a semiconductor memory taught in Yamaguchi. Applicant asserts that this substitution is improper.

First, Yamaguchi is directed towards solid state pick-up device such as those used in digital cameras. As the present invention is a video storage and distribution system, Yamaguchi is in a different field of endeavor than that of the present invention.

Second, Yamaguchi does not teach or suggest a memory that is relatively large by having an address bus that is more than 32 bits wide. Given that the standard processor was operating using a 32-bit bus, larger buses were not common. In addition, Yamaguchi specifically teaches away from using a relatively large memory in column 8, lines 33-38.

It is also important to recognize what the state of the art was in 2000 when this application was filed. Most off-the-shelf processors had 32 bit address buses. This limited the amount of semiconductor memory that they could access. See the present application, page 12, lines 5-9. This therefore limited the amount of content that was addressable by a CPU. To get around this problem, many content systems used disks like Rege. However, the use of disks introduced more latency in forwarding data to the users. This latency then limits the amount of users that can access content from a disk array at one time as well as the ability to write data into the disks in approximately the same time frame as data is being read from the disks.

These technological differences, coupled with the relative higher prices of semiconductor memory compared to disk memory, teach away from replacing Rege's disk memory with a semiconductor memory in 2000.

With respect to claim 29, Rege's CPU 310 does not serialize data as claimed and previously explained in relation to claim 28.

With respect to claim 31, the Examiner asserts that the server 300 of Rege includes an address generator. Applicant disagrees. As stated previously, there is no address bus between Rege's servers 300 and disks 800. Instead, arbiter 600 controls which lines are connected together between servers 300 and disks 800. See column 3, line 66 – column 4, line 1.

Also in rejecting claim 31, the Examiner adds the decoder 27 of Kondo to Rege, Rebec and Yamaguchi. Applicant asserts that this is an improper combination. Kondo's decoder 27 is in a client device such as receiver in a user's home. See column 11, lines 24-30. Rege is a system for delivering content. See generally the abstract. Thus, the

Examiner proposes to take a part from the client device of Kondo and add it to the server device of Rege. Applicant does not believe that the server device of Rege needs or would benefit from a component from a client device.

Claims not specifically mentioned above are allowable due to their dependency on an allowed base claim.

CONCLUSION

No fees beyond the Petition for a Three (3) Month Extension of Time are due for this response. However, the Office is authorized to charge any additional fees or underpayments of fees (including fees for petitions for extensions of time) under 37 C.F.R. 1.16 and 1.17 to account number 502117. Any overpayments should be credited to the same account.

Applicant respectfully requests reconsideration of the present application, withdrawal of the objections rejections made in the last Office Action and the issuance of a Notice of Allowance. The Applicant's representative can be reached at the below telephone number if the Examiner has any questions.

Respectfully submitted,

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__/Benjamin D. Driscoll/_____ __November 8, 2007___

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